THAT WHICH IS CLAIMED IS:

1. A method for making an electronic module comprising:

forming a low temperature co-fired ceramic (LTCC) substrate with at least one capacitive structure embedded therein by

arranging first and second unsintered ceramic layers and the at least one capacitive structure therebetween, the at least one capacitive structure comprising a pair of electrode layers, an inner dielectric layer between the pair of electrode layers, and at least one outer dielectric layer adjacent at least one of the electrode layers and opposite the inner dielectric layer, the at least one outer dielectric layer having a dielectric constant less than a dielectric constant of the inner dielectric layer, and

heating the unsintered ceramic layers and the at least one capacitive structure; and

mounting at least one electronic device on the LTCC substrate and electrically connected to the at least one embedded capacitive structure to form the electronic module.

2. The method of Claim 1 wherein the at least one outer dielectric layer comprises respective at least one outer dielectric layers adjacent each of the electrode layers and opposite the inner dielectric layer.

3. The method of Claim 2 wherein each at least one outer dielectric layer comprises a first outer dielectric layer and a second outer dielectric layer between the first outer dielectric layer and a respective electrode layer.

4. The method of Claim 3 wherein the second outer dielectric layer has a greater dielectric constant than a dielectric constant of the first outer dielectric layer.

5. The method of Claim 4 wherein the dielectric constant of the first outer dielectric layer is in a range of about 7-10, and the dielectric constant of the second outer dielectric layer is in a range of about 11-17.

6. The method of Claim 1 wherein the inner dielectric layer has a dielectric constant of greater than about 2000.

7. The method of Claim 1 wherein forming the LTCC substrate further comprises forming at least one signal trace adjacent the at least one outer dielectric layer.

8. The method of Claim 1 wherein the at least one outer dielectric layer and the inner dielectric layer each comprises less than about 15% by weight of glass.

9. The method of Claim 1 wherein the at least one outer dielectric layer comprises at least one of CaO, MgO, ZrO_2, BaO, and SiO_2.

10. The method of Claim 1 wherein the inner dielectric layer comprises $BaTiO_3$.

11. The method of Claim 1 wherein the electrode layers comprise at least one of Ag, Au, and AgPd.

12. The method of Claim 1 wherein the inner dielectric layer has a thickness of less than about 3 mils.

13. The method of Claim 1 further comprising forming conductive vias for electrically connecting the at least one electronic device and the at least one embedded capacitive structure.

14. The method of Claim 1 wherein the at least one capacitive structure has a capacitive density of greater than about 1000 pF/mm^2.

15. The method of Claim 1 wherein heating the unsintered ceramic layers and the at least one capacitive structure comprises heating at less than about 950°C.

16. A method for making an electronic module comprising:

forming a low temperature co-fired ceramic (LTCC) substrate with at least one capacitive structure embedded therein by

arranging first and second unsintered ceramic layers and the at least one capacitive structure therebetween, the at least one capacitive structure comprising a pair of electrode layers, an inner dielectric layer between the pair of electrode layers, a first outer dielectric layer adjacent at least one of the electrode layers and opposite the inner dielectric layer, and a second outer dielectric layer between the first outer dielectric layer and the at least one electrode layer, the inner dielectric layer having a greater dielectric constant than a dielectric constant of the second dielectric layer, and the dielectric constant of the second dielectric layer being greater than a dielectric constant of the first dielectric layer, and

heating the unsintered ceramic layers and the at least one capacitive structure; and

mounting at least one electronic device on the LTCC substrate and electrically connected to the at least one embedded capacitive structure to form the electronic module.

17. The method of Claim 16 wherein the first and second outer dielectric layers comprises respective first and second outer dielectric layers adjacent each of

the electrode layers and opposite the inner dielectric layer.

18. The method of Claim 16 wherein the dielectric constant of the first outer dielectric layer is in a range of about 7-10, and the dielectric constant of the second outer dielectric layer is in a range of about 11-17.

19. The method of Claim 16 wherein the inner dielectric layer has a dielectric constant of greater than about 2000.

20. The method of Claim 16 wherein forming the LTCC substrate further comprises forming at least one signal trace adjacent the first outer dielectric layer.

21. The method of Claim 16 wherein each of the first outer dielectric layer, the second outer dielectric layer, and the inner dielectric layer comprises less than about 15% by weight of glass.

22. The method of Claim 16 wherein each of the first and second outer dielectric layers comprises at least one of CaO, MgO, ZrO_2, BaO, and SiO_2.

23. The method of Claim 16 wherein the inner dielectric layer comprises $BaTiO_3$.

24. The method of Claim 16 wherein the electrode layers comprise at least one of Ag, Au, and AgPd.

25. The method of Claim 16 wherein the inner dielectric layer has a thickness of less than about 3 mils.

26. The method of Claim 16 further comprising forming conductive vias for electrically connecting the at least one electronic device and the at least one embedded capacitive structure.

27. The method of Claim 16 wherein the at least one capacitive structure has a capacitive density of greater than about 1000 pF/mm^2.

28. The method of Claim 16 wherein heating the unsintered ceramic layers and the at least one capacitive structure comprises heating at less than about 950°C.

29. An electronic module comprising:

a low temperature co-fired ceramic (LTCC) substrate;

at least one capacitive structure embedded in said LTCC substrate comprising a pair of electrode layers, an inner dielectric layer between said pair of electrode layers, and at least one outer dielectric layer adjacent at least one of said electrode layers and opposite said inner dielectric layer, said at least one outer dielectric layer having a dielectric constant less than a dielectric constant of said inner dielectric layer; and

at least one electronic device mounted on said LTCC substrate and electrically connected to said at least one embedded capacitive structure.

30. The electronic module of Claim 29 wherein said at least one outer dielectric layer comprises respective at least one outer dielectric layers adjacent each of said electrode layers and opposite said inner dielectric layer.

31. The electronic module of Claim 30 wherein each at least one outer dielectric layer comprises a first outer dielectric layer and a second outer dielectric layer between said first outer dielectric layer and a respective electrode layer.

32. The electronic module of Claim 31 wherein said second outer dielectric layer has a greater dielectric constant than a dielectric constant of said first outer dielectric layer.

33. The electronic module of Claim 32 wherein the dielectric constant of said first outer dielectric layer is in a range of about 7-10, and the dielectric constant of said second outer dielectric layer is in a range of about 11-17.

34. The electronic module of Claim 29 wherein said inner dielectric layer has a dielectric constant of greater than about 2000.

35. The electronic module of Claim 29 wherein said LTCC substrate further comprises at least one signal trace adjacent said at least one outer dielectric layer.

36. The electronic module of Claim 29 wherein said at least one outer dielectric layer and said inner dielectric layer each comprises less than about 15% by weight of glass.

37. The electronic module of Claim 29 wherein said at least one outer dielectric layer comprises at least one of CaO, MgO, ZrO_2, BaO, and SiO_2.

38. The electronic module of Claim 29 wherein said inner dielectric layer comprises $BaTiO_3$.

39. The electronic module of Claim 29 wherein said electrode layers comprise at least one of Ag, Au, and AgPd.

40. The electronic module of Claim 29 wherein said inner dielectric layer has a thickness of less than about 3 mils.

41. The electronic module of Claim 29 further comprising conductive vias for electrically connecting said at least one electronic device and said at least one embedded capacitive structure.

42. The electronic module of Claim 29 wherein said at least one capacitive structure has a capacitive density of greater than about 1000 pF/mm^2.